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TITLE: Method of manufacturing flash memory cell

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PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
KR 2003094442 A	December 12, 2003	N/A	001	H01L 021/8247

APPLICATION-DATA:

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ABSTRACTED-PUB-NO: KR2003094442A

BASIC-ABSTRACT:

NOVELTY - A method of manufacturing a flash memory cell is provided to prevent gathering effect by activating dopants implanted in the region in which an isolation layer is removed.

DETAILED DESCRIPTION - A trench-type isolation layer is formed at an isolation region of a semiconductor substrate such that the isolation layer has a protrusion. The first polysilicon layer(211) formed on the substrate is separated by the protrusion of the isolation layer. Subsequently, a dielectric layer(215), the second polysilicon layer(216), a silicide layer(217), and an anti-reflection layer(219) are formed over the semiconductor substrate. By removing the isolation layer and performing an ion implantation process, a common source line and a drain electrode are produced. A desired area of the common source line is locally annealed through a laser heating process.

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: METHOD MANUFACTURE FLASH MEMORY CELL

DERWENT-CLASS: L03 U11 U13 U14

CPI-CODES: L03-G04A; L04-C02B; L04-C10A; L04-C12C;

EPI-CODES: U11-C02J6; U11-C08A3; U11-C18B5; U13-C04B2; U14-A03B7;

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